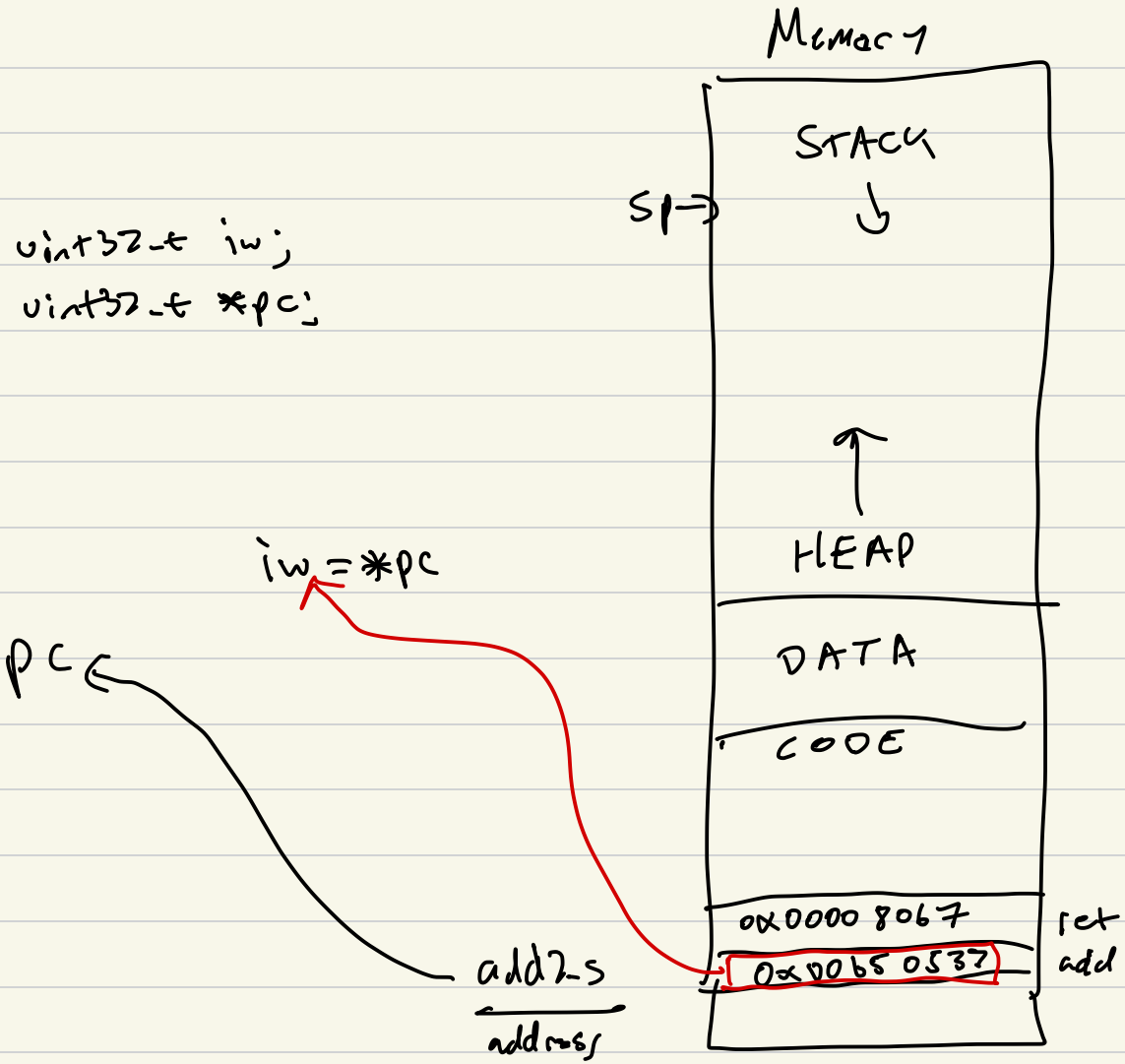
CS315-02 Lab RISC-V Machine Code

Lab03 Tue Oct 3
Project04 Tue Oct 10
IG Wed Oct 11
Midterm Thu Oct 12

Machine Code → Binary form of Assembly Language

1. RISC-V Emulator in C — Lab03 / Project04
2. Dynamic Analysis — Project04
3. Cache Simulation — Project04


Memory
STACK
SP
HEAP
DATA
CODE
uint32_t iw;
uint32_t *pc;
iw = *pc
pc
0x00008067
0x00050537
ret add
addr_s
address

add a0, a0, a1

0x00B50533

0000 0000 1011 0101 0000 0101 0011 0011

& mask

0000 ... zeros ... 0000 0111 1111

0000 ... 0000 0011 0011

opcode = 51

funct3 = 0

funct7 = 0

rd = 10

rs1 = 10

rs2 = 11

Emulation

uint64_t regs[32];